What is Claimed is:

1. A digital logic circuit comprising:

a first region of logic;

a second region of logic;

at least one pass transistor that is coupled between the first and second regions of logic and that has a gate terminal, wherein the pass transistor prevents digital signals from the first region of logic from passing to the second region of logic when the pass transistor is off and allows digital signals from the first region of logic to pass to the second region of logic when the pass transistor is on; and

control circuitry coupled to the gate terminal of the pass transistor for selectively turning the pass transistor off and on, wherein the control circuitry turns the pass transistor on by applying a power supply voltage to the gate terminal and turns the pass transistor off by applying a reverse-bias voltage to the gate terminal.

2. The digital logic circuit defined in claim 1 wherein the control circuitry comprises a configuration random-access memory cell.

3. The digital logic circuit defined in claim 1, wherein the digital logic circuit is an integrated circuit, the digital logic circuit further comprising a plurality of transistors each of which is turned on and off by the control circuitry using the power supply voltage and the reverse-bias voltage.

4. The digital logic circuit defined in claim 1 wherein the control circuitry comprises a configuration random-access memory cell having an output coupled to the control gate of the transistor and having a programming data input to which programming data is provided, wherein the programming data determines whether the output coupled to the control gate turns the transistor on or off.

5. The digital logic circuit defined in claim 1 further comprising:

a first pin for receiving a power supply voltage;

a second pin for receiving a ground voltage; and

charge pump circuitry that receives the power supply voltage and ground voltage and produces the reverse-bias voltage for the control circuitry.

6. The digital logic circuit defined in claim 1 wherein:

the digital logic circuit comprises a programmable logic device;

the control circuitry comprises a configuration random-access memory cell that is selectively configured depending on which programming data is loaded into the configuration random-access memory cell; and

the configuration random-access memory has cross-coupled inverters that store the programming

data, wherein the programming data is received from a data line that is selectively connected to the cross-coupled inverters in the random-access memory cell using an address line.

7. The digital logic circuit defined in claim 6 wherein the configuration random-access memory cell further comprises at least one transistor that is turned on with a power supply voltage and is turned off using a reverse-bias voltage.

8. The digital logic circuit defined in claim 1 wherein the transistor selectively connects two respective interconnection conductors located between the first and second logic regions.

9. An integrated circuit, comprising:

a plurality of transistors each having a gate terminal for controlling signal flow between first and second transistor terminals; and

a plurality of control circuits that each selectively apply to the gate terminal of a respective one of the transistors either a voltage supply signal to turn that respective transistor on or a reverse-bias voltage to turn that respective transistor off, wherein each transistor has a leakage current when turned off using the reverse-bias voltage that is lower than it would be if that transistor were turned off using a ground voltage, so that standby power consumption for the integrated circuit is reduced.

10. The integrated circuit defined in claim 9 further comprising programmable logic circuitry that is configured by selectively turning the transistors on or off in response to programming data.

11. The integrated circuit defined in claim 9 further comprising at least one multiplexer, wherein at least some of the transistors are included in the multiplexer and are selectively turned on an off in response to programming data used to configure the multiplexer.

12. The integrated circuit defined in claim 9 wherein each control circuit comprises a configuration random-access memory cell.

13. The integrated circuit defined in claim 12 wherein each configuration random-access memory cell has:

at least one input for receiving the power supply voltage;

at least one input for receiving the reverse-bias voltage;

a programming data input for receiving programming data that is stored in the configuration random-access memory cell; and

an output coupled to a corresponding one of the gate terminals that selectively applies to that control gate terminal either the power supply voltage or the reverse-bias voltage depending on which programming

data is stored in the configuration random-access memory cell.

14. The integrated circuit defined in claim 9 further comprising charge pump circuitry that generates the reverse-bias voltage from the power supply voltage and a ground voltage.

15. The integrated circuit defined in claim 9 further comprising additional transistors with gate terminals and additional control circuits each of which controls a respective one of the additional transistors by its gate terminal, wherein the additional transistors have higher threshold voltages than the plurality of transistors, and wherein the additional control circuits turn off their respective additional transistors by applying a ground voltage to their control gates.

16. A digital processing system comprising:

a processor;

a memory coupled to the processor; and

a programmable logic device coupled to the processor and the memory, the programmable logic device having:

a first region of logic;

a second region of logic;

at least one pass transistor coupled between the first and second regions of logic, wherein the pass transistor prevents digital signals from the first region of logic from passing to the second region of logic when the pass transistor is off and allows

digital signals from the first region of logic to pass to the second region of logic when the pass transistor is on; and

control circuitry coupled to a gate terminal of the pass transistor for selectively turning the pass transistor off and on, wherein the control circuitry turns the pass transistor on by applying a power supply voltage to the gate terminal and turns the pass transistor off by applying a reverse-bias voltage.

17. The digital processing system defined in claim 16 further comprising a circuit board on which the memory, the processor, and the programmable logic device are mounted.

18. The digital processing system defined in claim 16 further comprising input/output circuitry coupled to the programmable logic device, the processor, and the memory.

19. The digital processing system defined in claim 16 further comprising peripheral drivers coupled to the programmable logic device, the processor, and the memory.

20. The digital processing system defined in claim 16 wherein the control circuitry of the programmable logic device comprises a memory cell that stores programming data.

21. The digital processing system defined in claim 16 wherein the programmable logic device further comprises:

a first pin for receiving a power supply voltage;

a second pin for receiving a ground voltage; and

charge pump circuitry that receives the power supply voltage and ground voltage and produces the reverse-bias voltage.